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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MAI, SON LUU

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/896,446

Applicant(s)

SRINIVASAN ET AL.

Examiner

Son L. Mai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27-29 is/are allowed.
- 6) ☒ Claim(s) 1-26 and 30-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

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### DETAILED ACTION

1. The amendment filed on 07-29-02 has been entered. Claims 1-33 are pending in the application.

#### *Drawings*

2. The substitute drawings were received on 07-29-02. These drawings are accepted by the Examiner.

#### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 30-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 30, lines 5-6, the recitation "a first drain bias network coupled to the kicker circuit; a second drain bias network coupled to the reference kicker circuit" is misdescriptive. Since the kicker circuit is a part of the first drain bias network, by claiming "a first drain bias network coupled to the kicker circuit" the Applicants claim the first drain bias network and the kicker circuit are independent elements. Similarly, a correction should be made to the second drain bias network.

Claims 31-33 are rejected for incorporating the limitations of claim 30.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-26 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent 5,559,737).

The Tanaka et al. patent discloses all the limitations as claimed in the instant invention. In the embodiment illustrated in figure 2, Tanaka et al. shows a flash cell (transistor 1) coupled to a first drain bias network (comprising of elements 4-7), a reference cell (11) coupled to a second drain bias network (comprising of elements 14-17), a single equalizing transistor (91) coupled to input nodes of the first and second drain bias networks for equalizing the potential thereof, and a sense amplifier (20) coupled to the outputs of the first and second drain bias networks. The method claims of the instant invention read on the circuitry of Tanaka et al. comprising equalizing input nodes of the first and second drain bias networks and sensing the voltage difference between the outputs of the first and second drain bias networks.

The newly added claim 30 is anticipated by the Tanaka et al. patent. In figure 2, Tanaka et al. shows an apparatus comprising: a reference cell (111), a first drain bias network with a kicker circuit (4-7), a second drain bias network with a reference kicker circuit (14-17), a sense amplifier (20) and a single equalizing transistor (91) coupled between an input of the kicker circuit and an input of the reference kicker circuit.

***Allowable Subject Matter***

6. Claims 27-29 are allowed.

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7. Claims 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the detail limitations of the kicker circuit as claimed in claim 27 which calls for a kicker circuit including: a first transistor having a first node, a second node and a gate node, the first transistor coupled at its first node to a gate node of a second transistor, to a first node of a third transistor, and to a gate node of a fourth transistor, the first transistor coupled at its second node to ground, and the first transistor coupled at its gate node to a first node of the equalizing transistor and to a first node of the second transistor the second transistor having a second node, the second transistor coupled at its second node to the first node of the fourth transistor and to the first drain bias network; the third transistor having a second node and a gate node, the third transistor coupled at its second node to a power supply, and the third transistor coupled at its gate node to the power supply; and the fourth transistor having a second node, the fourth transistor coupled at its second node to the power supply.

### ***Response to Arguments***

9. Applicant's arguments filed 07-29-02 have been fully considered but they are not persuasive.

In the Remarks on page 18, the Applicants contend that (1) Tanaka equalizes the potential between a cell and a dummy cell at two points; thus Tanaka utilizes 3

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equalizing transistors versus a single equalizing transistor as in the presently claimed invention, and (2) the presently claimed invention is directed to FLASH memory devices not the EPROM devices referenced by Tanaka.

In response to the first point (1), the Examiner would like to direct the Applicant to figure 2 of the Tanaka et al. reference. In the figure, transistor 91 corresponds to the single equalizing transistor for equalizing the potential of the first and the second drain bias networks as claimed. On the contrary, transistors 92 and 93 make up another equalizing circuit for equalizing the potential of the sense line and the dummy cell sense line. See column 5, lines 39-56.

To the second point (2), the Tanaka et al. reference discloses at column 9, line 61 through column 10, line 3, that the disclosed apparatus can be applied to not only an EPROM but also to an EEPROM. But it is known in the memory art that a FLASH memory device is an EEPROM memory device having a flash erase mode. Therefore, the Tanaka et al. reference is also applied to a flash memory device.

### **Conclusion**

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 305-3497. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

10-02-2002



Son Mai  
Patent Examiner  
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